p-channel typ MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

10. (Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

11. (Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region.

Please add the following new claims:

39. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes an MIS transistor to which a substrate bias is appli d in a reverse

direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

A2 Cont.

40. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

41. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

42. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to